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# Performance evaluation of systematic and nonsystematic polar encoding using FPGA under a practical multipath channel

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**Abstract**

Polar code is currently implemented in high-speed high performance modern communication systems. The polar code enabled these systems to transmit near Shannon's limit with minimum bit error rate (BER). However, the performance of polar encoding is enhanced using a systematic encoding technique that convolves the data, providing higher noise immunity. This paper provides the hardware implementation of systematic and nonsystematic encoding using an FPGA to provide fully parallel operation for maximum processing speed. Both techniques' performance is evaluated under the additive white Gaussian noise (AWGN) channel and a practical indoor multipath channel. Both techniques showed a significant BER improvement compared to BPSK. The tests showed that the systematic performance is superior to the nonsystematic technique.



*Keywords*: Channel polarization, Polar code, Encoding and decoding, High-speed transmission

## 1. Introduction

High-speed communication has become an essential necessity in the modern lifestyle. Therefore, new coding techniques were developed to fulfill the needs for such speeds required by the latest communication systems, such as 5 5G. One of the prominent coding schemes that attracted the attention of the developers is the polar coding that guarantees a near-Shannon channel capacity speed limit. Erdal Arikan is credited with introducing polar codes in his paper in 2009 [1]. His work provided rigorous mathematical proof that these codes can achieve channel capacity, a significant milestone in coding theory. Arikan relied on the concept of channel polarization to create the polar code. The fundamental idea is based on dividing the channel through which data is transmitted into several sub-channels.

This division is done through precise mathematical calculations. The sub-channels are divided into more reliable and less reliable parts [2-4]. Data is transmitted through the more reliable channels, while the rest are neglected by assuming them as frozen data and always equaling zero. Polar codes have unique properties that distinguish them from other codes. They are characterized by a simple and clear structure, making them easy to implement in many current and future applications. This paper presents the hardware implementation of polar coder/decoder circuits using a field programmable gate array (FGPA) [5]. For instance, a code (16, 8) will be adopted for implementation. The paper organization is: Section II gives the theoretical concepts of

nonsystematic polar code, Section III explains how to apply the systematic algorithm to nonsystematic polar code, and we will also explain the decoding process of polar code, the communication system details, and the system construction.

The polarization of the channel is the cornerstone of polar codes, enabling them to achieve the Shannon-Hartley theorem and make them the best-performing error-correcting code. In information theory, Shannon defines the capacity of any channel as the maximum baud rate at which data can be transmitted over a corrupted channel with high reliability, with no errors. The mathematical expression for channel capacity is written as (1) [6, 7]:

$$\mathrm{C} = \mathrm{B}\log_2\left(1+\frac{S}{N}\right) \tag{1}$$

Where: *C*: is the capacity of the channel, *B*: is the channel's bandwidth, and $\frac{S}{N}$ : is the transmitted signal power to noise power ratio.

The fundamental concept of channel polarization lies in dividing the main channel into sub-channels *N* with varying capacities *I(C)*. Some of these sub-channels are considered good and suitable for data transmission due to their extremely low noise ratio compared to others, which are considered bad for information transmission, leading to a high probability of errors. Therefore, data will be sent through good channels without errors, while bad channels will be neglected. A binary-input memoryless channel (B-DMC) serves as a fundamental model for understanding channel polarization.

In this channel $C:\mathrm{X}\to\mathrm{Y}$ , the input $x\in\mathrm{X}$ and output $y\in\mathrm{Y}$ where $x\{0,1\}$ over linear *GF*(2), and the errors introduced during transmission are independent of each other.

Let *N* represent the number of copies of the channel, $C^N:\mathrm{X}^N\to\mathrm{Y}^N$ with transition probabilities. The two important factors to measure of rate and reliability to achieve channel polarization [1, 8]; the symmetric capacity as in (2) and the Bhattacharyya parameter as in (3).

$$I(C)=\sum_{y\in\mathrm{Y}}\sum_{x\in\mathrm{X}}\tfrac{1}{2}\,C(y\mid x)\log\left(\frac{C(y\mid x)}{\frac{1}{2}\,C(y\mid 0)+\frac{1}{2}\,C(y\mid 1)}\right) \tag{2}$$

$$\mathrm{Z}(C)\square\sum_{y\in\mathrm{Y}}\sqrt{C(y\mid 0)\,C(y\mid 1)} \tag{3}$$

For any B-DMC *C*, the relation between these two parameters can be written as in (4) [9]

$$I(C)\le\sqrt{1-\mathrm{Z}(C)^2} \tag{4}$$

The polar coding scheme commences with the utilization of a fundamental polarization kernel. Polar coding transmission technique as shown in Figure 1.

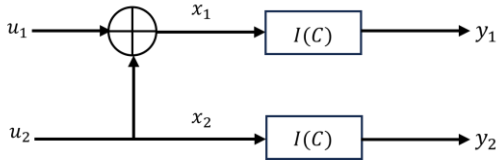



Figure 1. Polar coding transmission technique

The input vector $u_1^N$ is permuted by the matrix $B_N$ . where $B_N=R_N\left(I_2\otimes B_{N/2}\right)$, $I_2$ is $(2\times 2)$ identity matrix and $R_N$ is used for index reordering as in $[u_1,u_2,\cdots,u_N]\times R_N=[u_o,u_e]$ where o = 1, 3, 5, … and e= 2, 4, 6, … By multiplying the generator matrix $\mathrm{S}^{\otimes n}$ with $n^{th}$ Kronecker power yields (5):

$$x_1^N = u_1^N B_N \mathsf{S}^{\otimes n} \tag{5}$$

In polar code, $\mathsf{S}_N$ is the kernel matrix, which characterizes the encoding transformation $\mathsf{S}_2$. More specifically, the kernel $\mathsf{S}_2$ may be represented as in the Equation (6):

$$\mathsf{S}_2 = \begin{pmatrix} 1 & 0 \\ 1 & 1 \end{pmatrix} \tag{6}$$

While the *N-bit* encoder $\mathsf{S}_2$ is defined recursively as in (7):

$$\mathsf{S}_N = \mathsf{S}_2^{\otimes n} = \begin{pmatrix} \mathsf{S}_{N/2} & 0 \\ \mathsf{S}_{N/2} & \mathsf{S}_{N/2} \end{pmatrix} \tag{7}$$

The encoding process of polar code [10], which was generalized for an arbitrary encoder. Based on Figure 1, an encoder circuit can be designed for any given $N$ number of channels. Let $K$ represent the length of information bits sent through the perfect channels. In the process of channel polarization, $k = N \times I(C)$ represents the good channels, which are suitable for data transmission. In contrast, $(N - k)$ or $N \times (1 - I(C))$ represents the bad channels, through which no data is transmitted. These channels are always 0 and are referred to as frozen channels. As a result, the code rate is designed to match the channel capacity of the communication system. This means that the code can be used for the maximum possible rate transmission without causing errors, ensuring efficient and reliable received data as in (8):

$$R = \frac{K}{N} = \frac{(N \times I(C))}{N} = I(C) \tag{8}$$

The encoding process may be represented as shown in Figure 4 for $N = 8$.

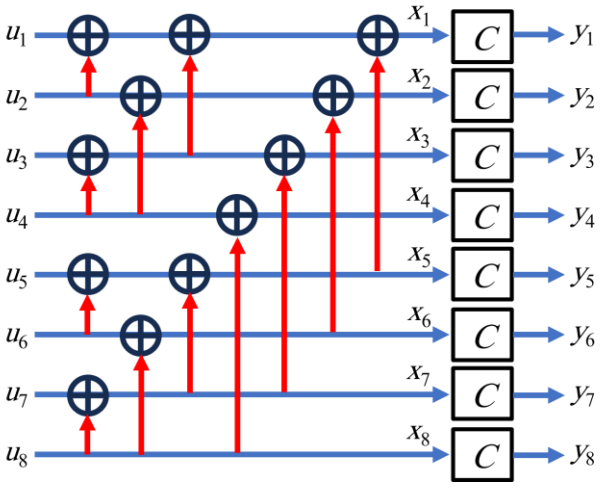



Figure 2. The polar process for $N = 8$

In a non-systematic polar code, the input data vector as $\mu$ and the code word as $x$, while for a systematic polar code, the vector $\mu$ is subdivided into data and frozen bits parts $\mu = (\mu_A, \mu_{Ac})$, where $A \subset \{1,\ldots,N\}$, $\mu_A = \mu_i : i \in A$ contains information bits while $\mu_{Ac} = (\mu_i : i \in A_c)$ represents the frozen bits recognized by the decoder. The vector of the codeword is given by (9):

$$x = \mu_A \mathsf{S}_A + \mu_{Ac} \mathsf{S}_{Ac} \tag{9}$$

Where $\mathsf{S}_{\mathrm{A}}$ and $\mathsf{S}_{\mathrm{A}c}$ are represent subarrays of $\mathsf{S}$ defined in (5) , for a systematic polar code, the code word vector, a random subset of bits $\{1,\ldots,N\}$ represents the *B* and can be rewritten as in (10) [11]:

$$\begin{aligned} x_B &= \mu_{\mathrm{A}}\mathsf{S}_{\mathrm{A}B} + \mu_{\mathrm{A}c}\mathsf{S}_{\mathrm{A}cB} \\ x_{Bc} &= \mu_{\mathrm{A}}\mathsf{S}_{\mathrm{A}Bc} + \mu_{\mathrm{A}c}\mathsf{S}_{\mathrm{A}cBc} \end{aligned} \tag{10}$$

Decoding in polar codes is the process of recovering the original message from a received codeword that may have been corrupted by noise or errors during transmission. Therefore, must be considered when selecting an appropriate algorithm for polar code decoding, such as High error correction efficiency, Code length, Circuit structure complexity, and information recovery time. Balancing these factors is crucial for selecting the most suitable decoding algorithm for a specific application. The basic decoding algorithm is a successive cancellation decoder (SCD) for polar code. This method is considered the fundamental and very widely used approach for decoding polar codes [12]. It is simple to implement and offers good performance for short codewords. Its operation principle is based on iteration, starting from the most reliable bit to the least reliable bit based on the received data. In each step, a decision is made about the bit, and then the information for the other bits is updated. In real-time applications, the successive cancellation (SC) decoder is often preferred due to its ease of representation. The implementation of an SC decoder circuit closely resembles that of a polar code encoder, but the computations differ. In the encoder, calculations proceed from left to right, while in the SC decoder, they are performed in the opposite direction. The polar decoder circuit contains (*n*) stages and (*N*) levels. Each stage consists of $N/2$ butterfly sections. The SC decoding process initiates with the availability of Log-Likelihood Ratio (*LLRs*) values on the right side of the circuit. These values are denoted by $R_{i,j}$ are the received signal after passing through the channel provided by the soft demodulator, where $(1 \le i \le N, 1 \le j \le n+1)$. The operation of each XOR gate in the decoder circuit depends on a sequence of steps in the SC decoder. The XOR gates perform three different computational processes depending on the *LLR* values or bit values. The computational processes of the XOR gates are given in (11) [13]:

$$\begin{aligned} R_{i,j} &= f\,(R_{i,j+1}, R_{i+2^{j-1},j+1}) \\ R_{i,j} &\approx \mathrm{sgm}(R_{i,j+1}) \cdot \mathrm{sgm}(R_{i+2^{j-1},j+1}) \cdot \min(\left|R_{i,j+1}\right|, \left|R_{i+2^{j-1},j+1}\right|) \end{aligned} \tag{11}$$

Where sgm (·) is the signum, which is –1 if the argument is negative and +1 if positive as in (12):

$$R_{i+2^{j-1},j} = g\,(R_{i,j+1}, R_{i+2^{j-1},j+1}, \breve{\mathrm{B}}_{i,j}) = (-1)^{\breve{\mathrm{B}}_{i,j}} R_{i,j+1} + R_{i+2^{j-1},j+1} \tag{12}$$

The sign of $\left(R_{i+2^{j-1},j}\right)$ will dictate whether the bit $\left(\breve{\mathrm{B}}_{i,j}\right)$ is assigned a value of zero or one after that it will be possible to obtain both values subsequently $\left(\breve{\mathrm{B}}_{i,j+1}, \breve{\mathrm{B}}_{i+2^{j-1},j}\right)$ as in (13):

$$\begin{aligned} \breve{\mathrm{B}}_{i,j+1} &= \mathrm{XOR}(\breve{\mathrm{B}}_{i,j}, \breve{\mathrm{B}}_{i+2^{j-1},j}) \\ \breve{\mathrm{B}}_{i+2^{j-1},j+1} &= \breve{\mathrm{B}}_{i+2^{j-1},j} \end{aligned} \tag{13}$$

### 1.1. The system description

MATLAB System Generator will be implemented to create an FPGA model for the polar code circuit. The nonsystematic and systematic polar code encoder circuits BER will be implemented and compared to the uncoded BPSK to evaluate their performance.

### 1.2. Binary phase-shift keying (BPSK) circuit

Binary phase-shift keying (BPSK) transmits bi-phase signal where 1 is transmitted as – 1 and 0 as 1 [14]. The BPSK modulator circuit (Figure 3) consists of a selector and a comparator to choose the level for the bits coming from the polar encoder circuit. The comparator compares the bit to 0, and if it is 0 the selector output will be 1 and the d1 pin is selected, which is connected to the +1 level. Otherwise, -1 is selected when the bit = 1. The receiver circuit compares the noisy received signal to the 0 level. If the received signal is less than 0, then it is possibly that the bit =1 while if it is equal or higher than 0, then the bit = 0 as shown in Figure 4.

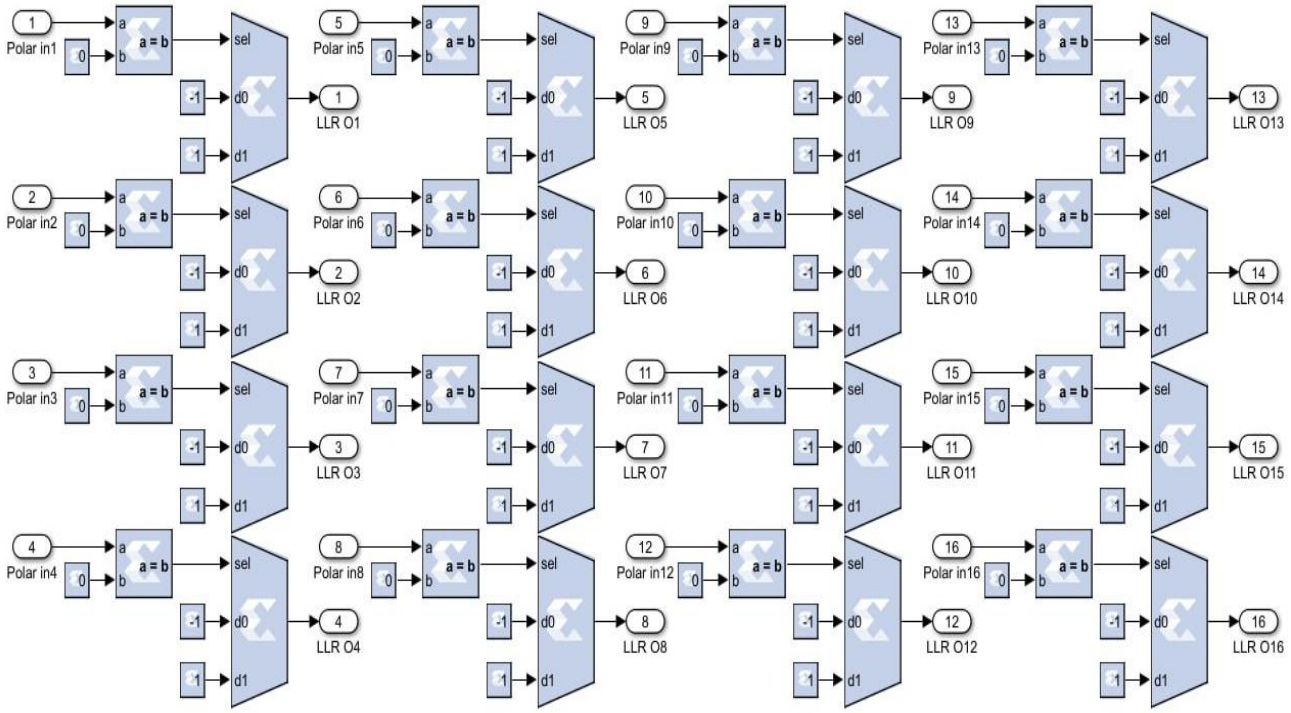



Figure 3. The BPSK modulator

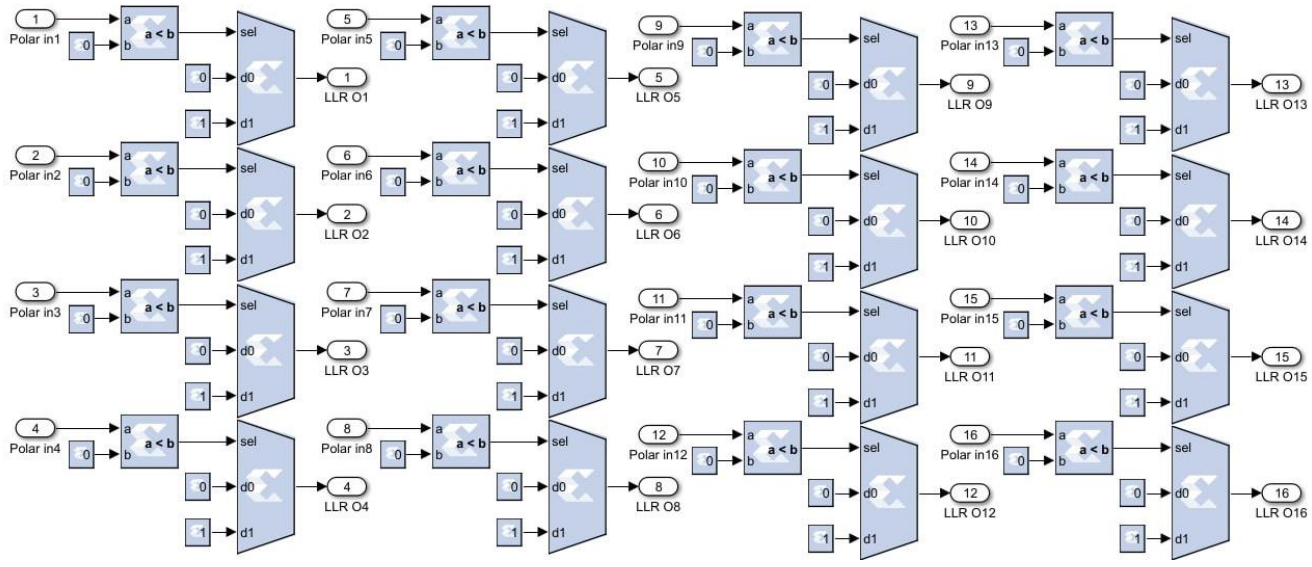



Figure 4. The BPSK demodulator

## 2. The channel model

The polar code performance will be evaluated by transmitting data through a practical indoor multipath channel as shown in Figure 5 [15]. At the receiver, the compensation for counteracting the influence of the multipath circuit is shown in Figure 6, which is the inversion of the channel response.

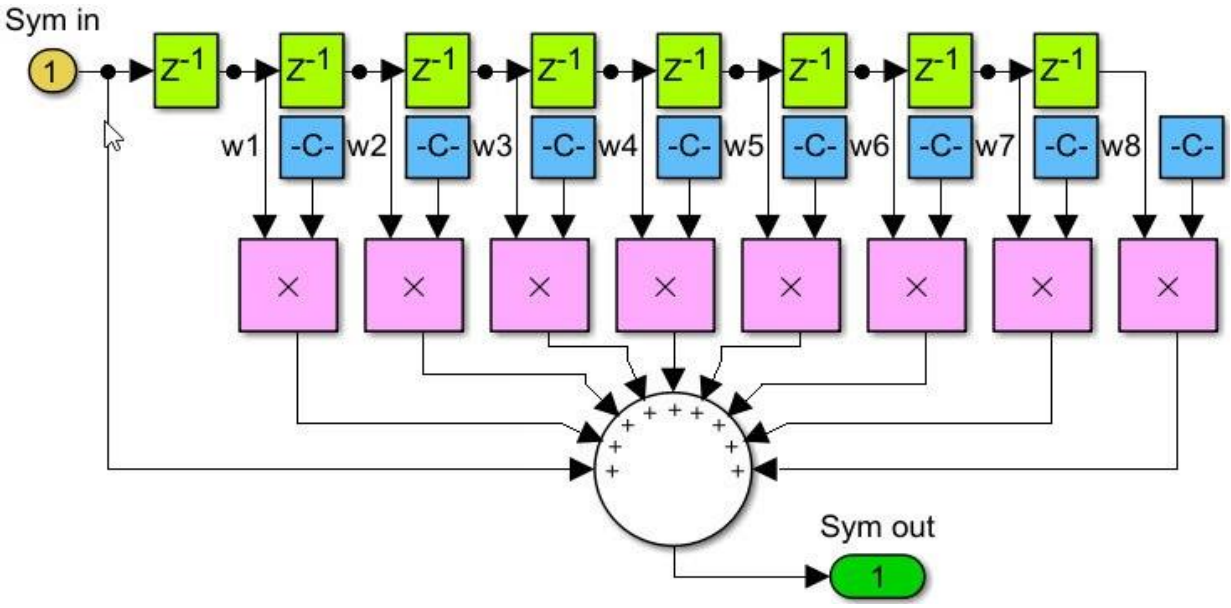



Figure 5. The indoor multipath channel

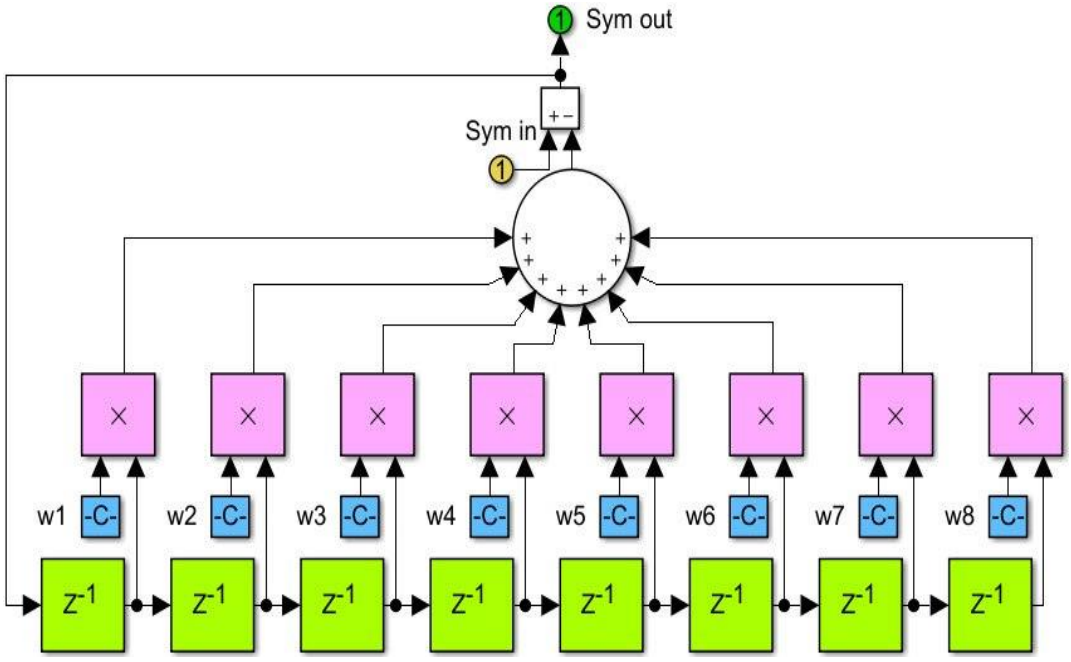



Figure 6. The compensation circuit for the multipath indoor channel

Xilinx System Generator will be employed to construct a hardware implementation of a polar code encoder. The circuit shown in Figure 2 is to be implemented in hardware using a configuration of XOR gates, with N=16, as shown in Figure 7.

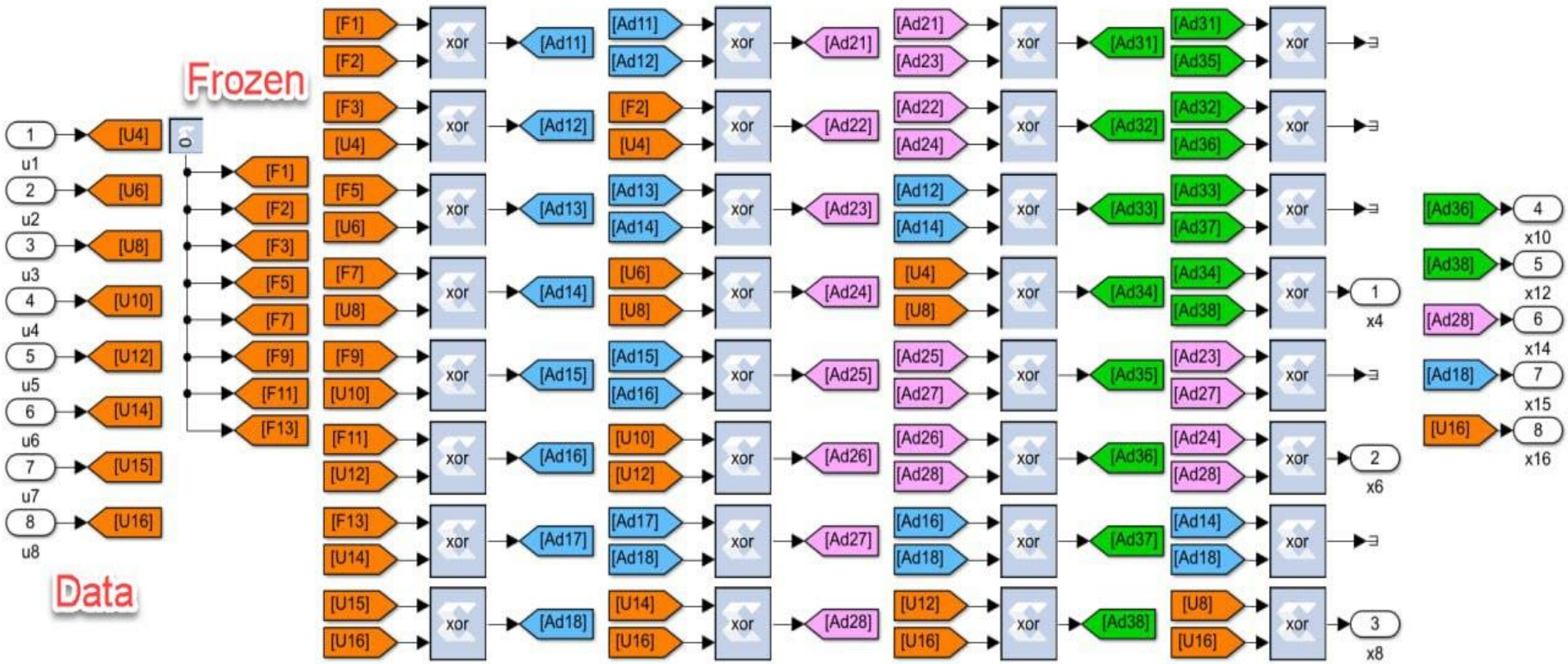



Figure 7. Nonsystematic polar encoder circuit

The core of the polar code decoding process is based on Equations 11 and 12. These equations will be implemented in hardware using Xilinx blocks, as shown in Figure 8.

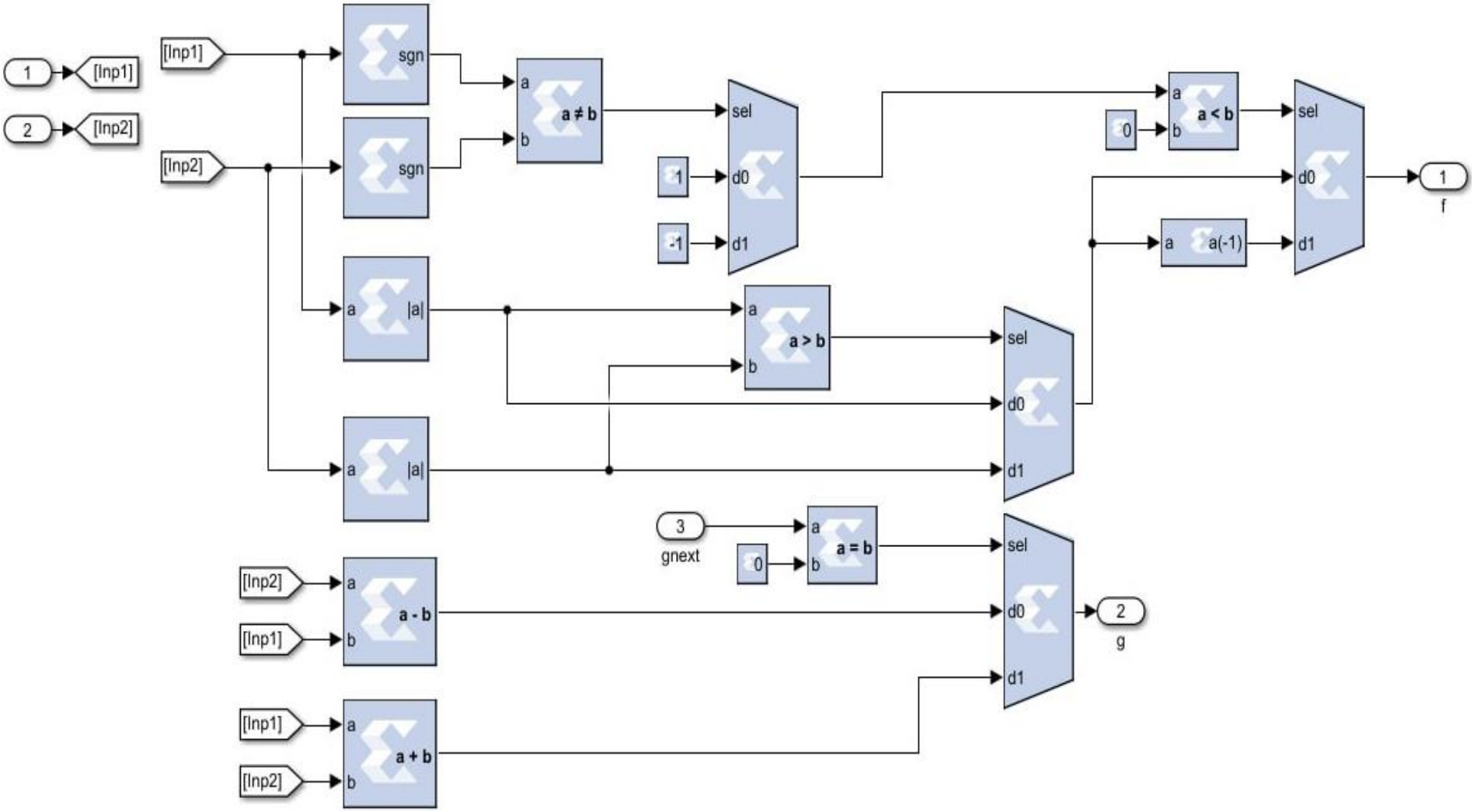



Figure 8. The model for f () and g () of polar decoder

The decoder circuit, as illustrated in Figure 9, will be constructed where each block contains the *f* and *g* equations previously described in Figure 8. The circuit will be designed for $N = 16$.

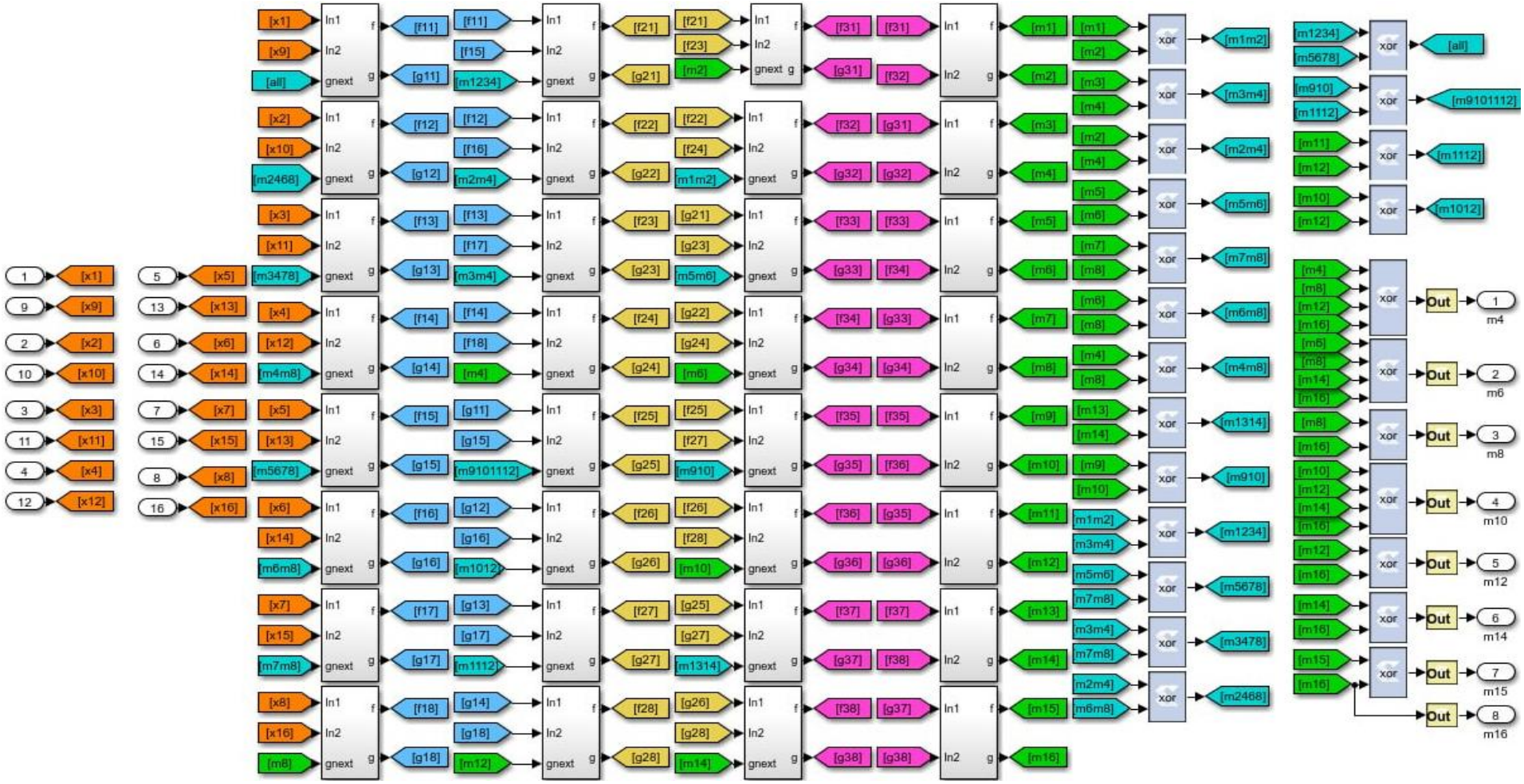


Figure 9. The polar successive cancellation (SC) decoder circuit

## 3. Results and discussion

Previously detailed components are connected to build a transmission system. The bits will be generated using Simulink's Bernoulli block, fed to the polar encoder, and modulated by a BPSK modulator. Initially, the system will be tested under an AWGN channel without polar encoding or multipath channel as shown in Fig.10 to establish the BER reference performance.

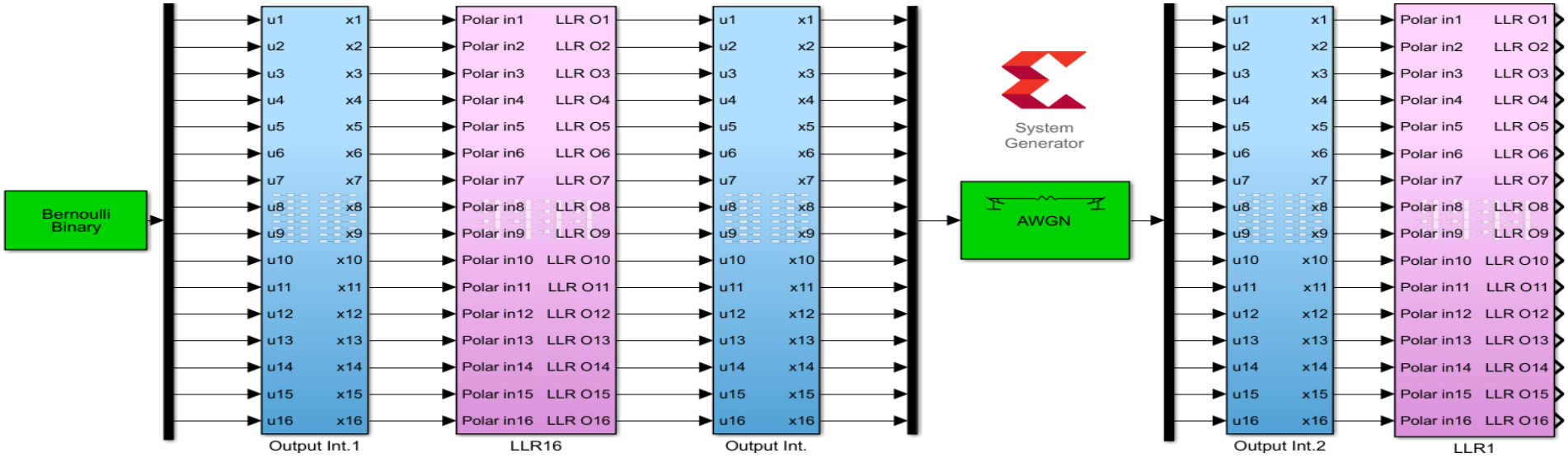



Figure 10. The FPGA model for the BPSK modulator and demodulator with AWGN channel

The second test will include the nonsystematic polar encoder/decoder circuit as shown in Figure 10.

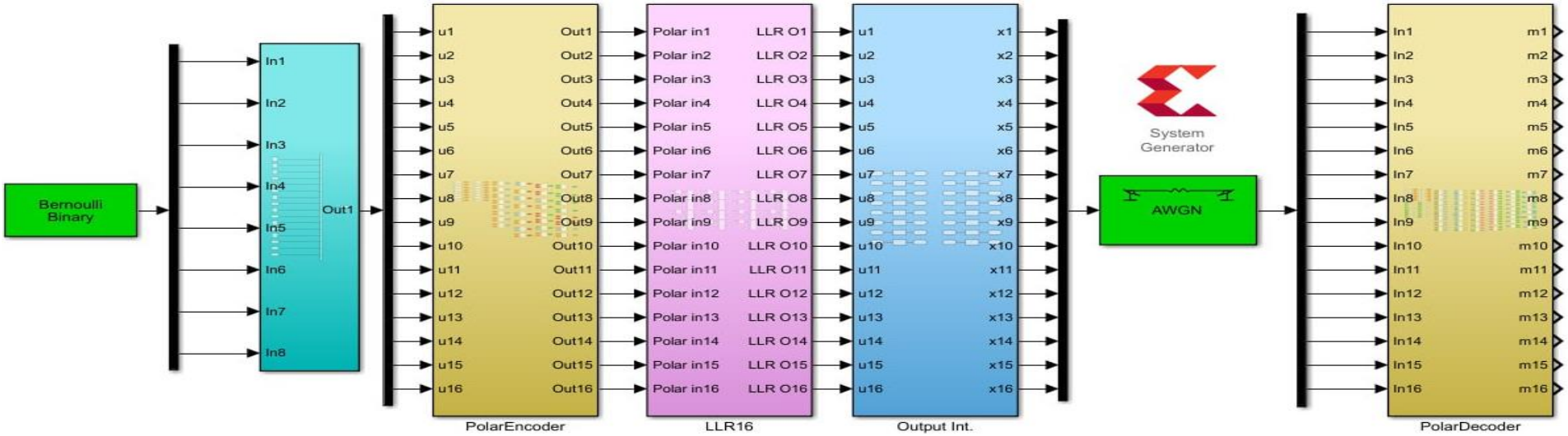



Figure 11. The FPGA Model for the nonsystematic Polar Encoder and SC Decoder with AWGN channel.

The third test will be for the systematic polar encoder/decoder circuit as shown in Figure 12.

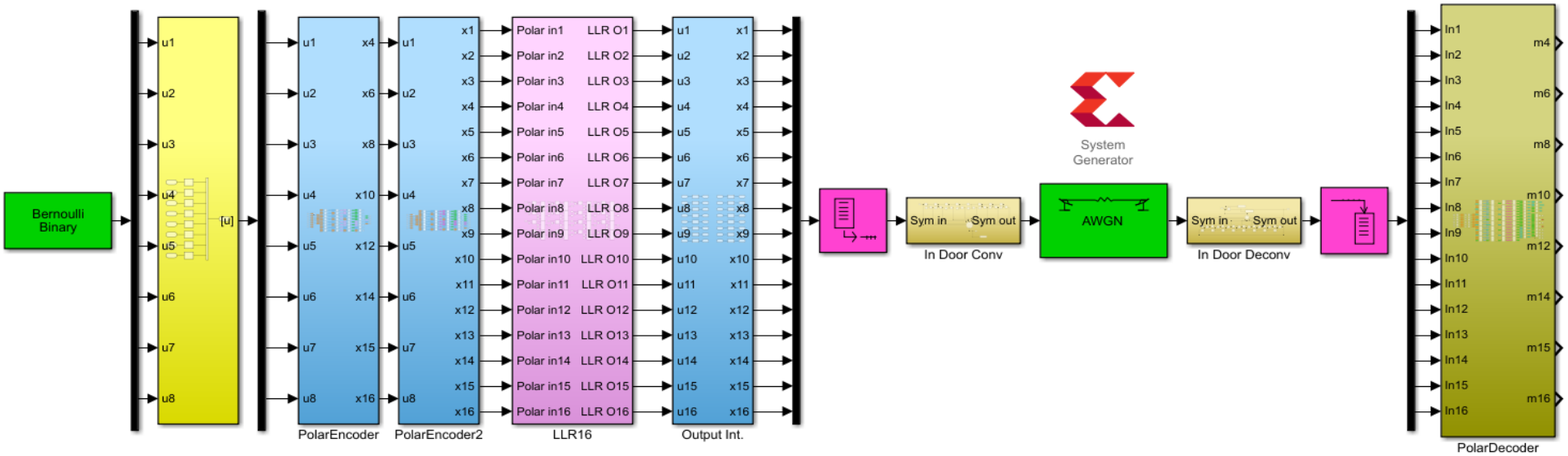



Figure 12. The FPGA Model for the systematic Polar Encoder and SC Decoder with AWGN channel

The other tests will include the multipath indoor channel. The first test will be the multipath uncoded BPSK as shown in Figure 13.

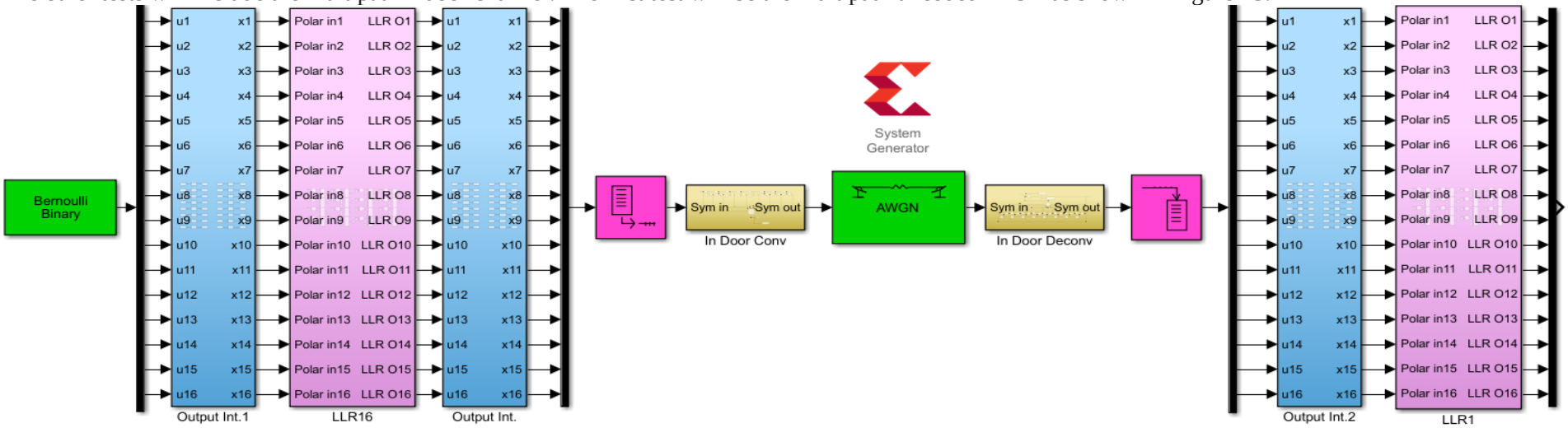



Figure 13. The FPGA model for the BPSK modulator and demodulator with a multipath indoor channel

The second test will be for the nonsystematic polar coder/decoder as illustrated by Figure 14.

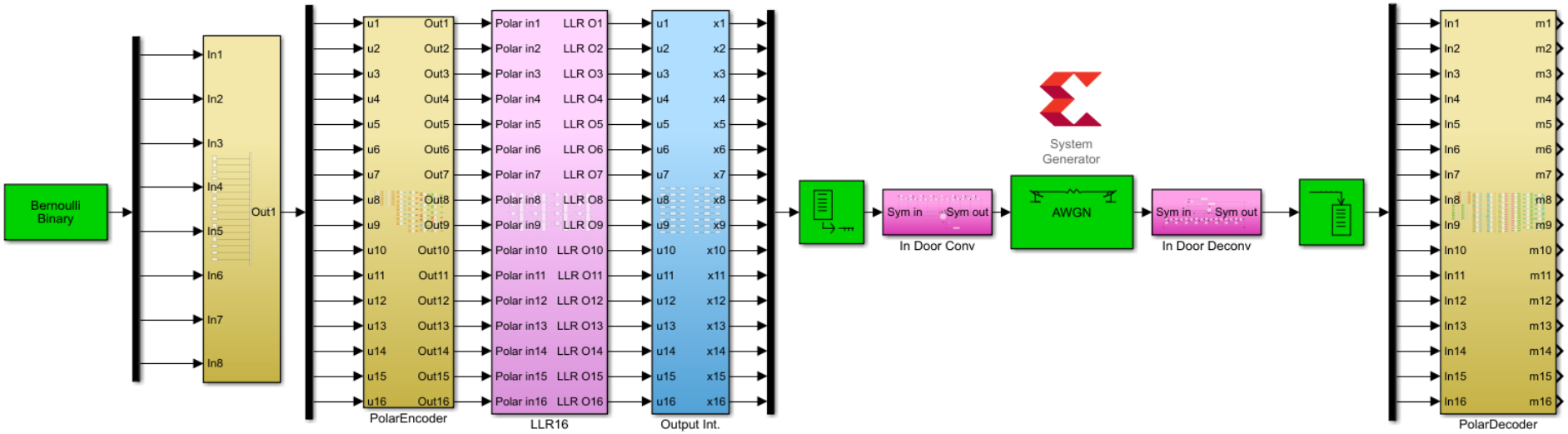



Figure 14. The FPGA model for the nonsystematic polar encoder and SC decoder with a multipath indoor channel

The third test will be for the systematic polar encoder/decoder as shown in Figure 15.

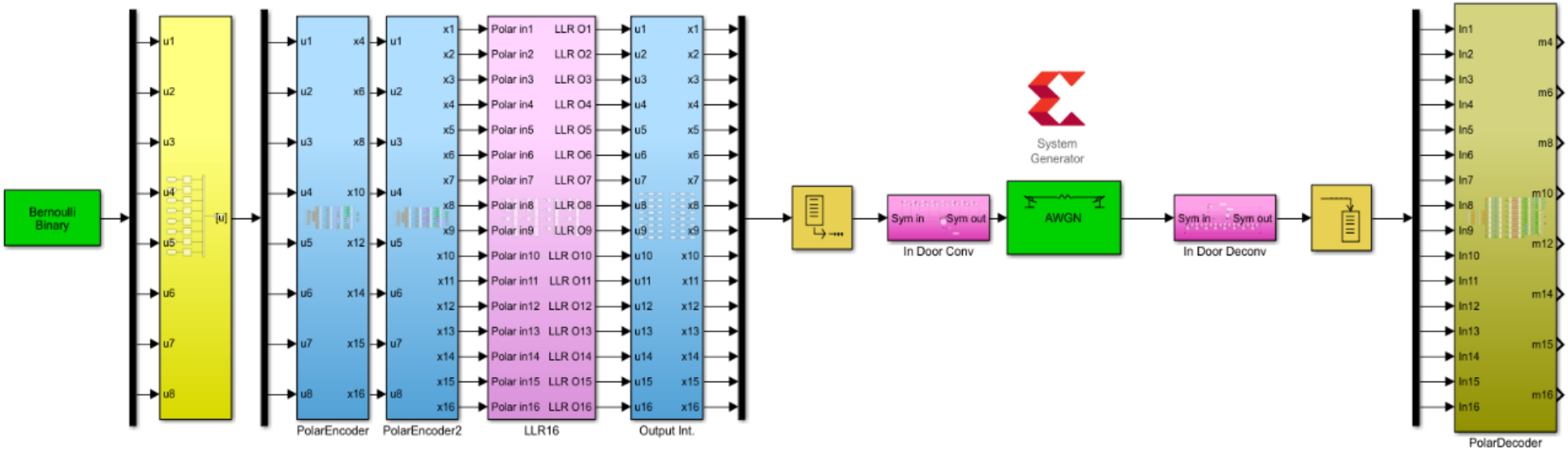
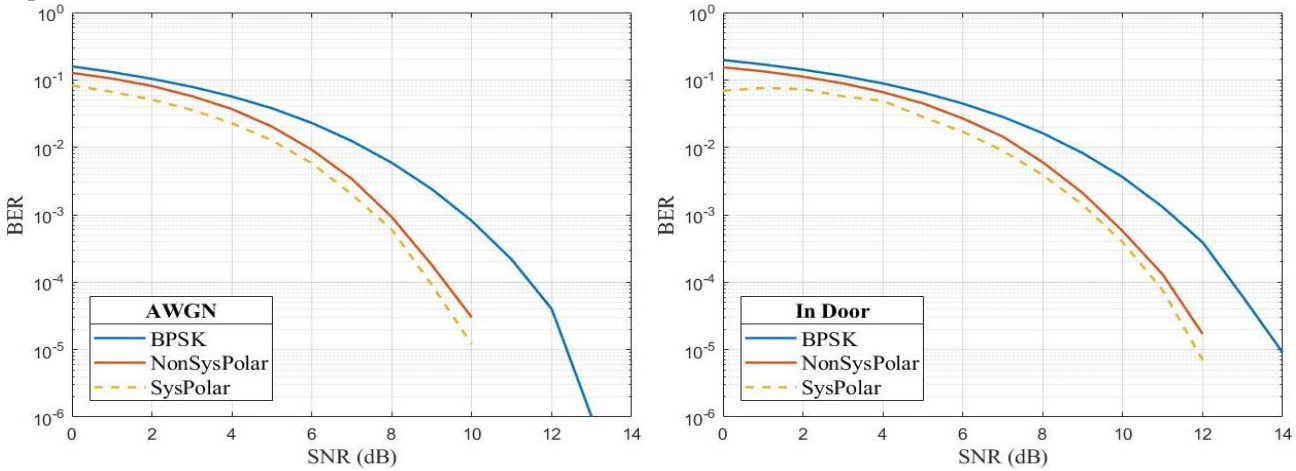



Figure 15. The FPGA model for the systematic polar encoder and SC decoder with a multipath indoor channel

The test is performed by sending at least $10^6$ bits, and the results are shown in Figure 16a for the AWGN and 16b for the multi-path channel. The results show that the polar code, nonsystematic and systematic, performs better than the uncoded BPSK. The nonsystematic and systematic BER are better than the uncoded BPSK by 1.8 and 2.2 dB, respectively. This means the systematic upgrade gave about 0.4 dB. These findings can be exploited in [16-27] as future trends.




(a) (b)

Figure 16. The BER Results of the uncoded BPSK, Nonsystematic and systematic polar code (a) AWGN, (b) Indoor multipath channel

## 4. Conclusion

The polar code is a very efficient technique that combines simplicity with the BER performance improvement. The polar enables the communication system to transmit near Shannon's channel limit to qualify the system to handle massive data loads with high transmission speed. The nonsystematic polar code can be improved by implementing the systematic technique. The amount of SNR improvement is about 0.4 dB. By comparing the increased system complexity to the SNR improvement, it can be seen that the system is worthy of practical implementation.

The FPGA is selected for the polar implementation because the FPGA provides a pure parallel processing environment. The implementation of the polar code using the steps given in this paper shows that the polar code can be used in parallel processing environments, which highly improves its speed and reduces the time delay. The polar code circuits given in this paper show how simple it is to construct the polar encoder/decoder for both systematic and nonsystematic codes using only logic gates and switches. Testing the FPGA polar system proves that the final system is operational without any problems or hardware glitches.

### Declaration of competing interest

The authors declare that they have no known financial or non-financial competing interests in any material discussed in this paper.

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### Author contribution

Ghadeer H. Eskandar and Samir J. Mohammed contributed equally to this work. Ghadeer H. Eskandar was responsible for the conceptualization of the study, designing the experiments, and conducting the simulations. Samir J. Mohammed contributed to the development of the FPGA implementation, data analysis, and

interpretation of results. Both authors collaborated on writing and revising the manuscript, ensuring that all aspects of the research were accurately represented and discussed. They also jointly addressed feedback from peer reviews and finalized the submission of the manuscript.

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